Single Photon Avalanche Diodes (SPADs) for 1.5 µm Photon Counting Applications

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Presentation Outline

- InGaAs/InP SPAD design strategy
  - Differences between SPADs and APDs
- SPAD performance and wafer-level variation
  - Modest structural differences introduce significant performance shifts
- Afterpulsing and carrier trapping
  - Modeling for characteristic de-trap times
  - Extraction of de-trapping thermal activation energy
- Activation energy for dark count rates
- Timing jitter behavior
- Conclusions
InGaAs/InP Avalanche Diode Design Platform

- Separate Absorption, Charge, and Multiplication (SACM) structure
  - Maintain high E-field in multiplication region to induce avalanching
  - Maintain low E-field in absorption region to suppress tunnel current

- Planar passivated, dopant diffused device structure
  - Junction profile shaping to suppress edge breakdown
  - Highly stable and reliable performance for buried p-n junction
  - Platform proven through widespread deployment in telecom receivers
Linear Mode vs Geiger Mode (APDs vs SPADs)

- Linear Mode APDs should achieve an optimal E-field profile below breakdown (M ~ 10 - 20)
- For SPADs, optimal E-field profile needed at target overbias
- A good APD will have excessively large absorption region E-fields if operated as a SPAD
  - Other layers may also be non-optimal (e.g., multiplication region width)
- What has to “go wrong” with an APD to get a good SPAD?
  - If thickness and doping levels are higher than APD targets, increased field control charge may give E-fields appropriate for good SPAD performance
  - Certain screening parameters may serve to identify potential SPAD devices (e.g., elevated breakdown voltage), but works only for specific variations
  - Screening is not a good strategy for manufacturing SPADs!
Linear Mode as Indicator of SPC Performance

- I-V characteristics in linear mode below breakdown - what matters for SPADs?
  - Weak V-dependence indicates unmultiplied perimeter leakage; bulk leakage will exhibit linear mode avalanche gain
  - Only bulk leakage contributes to DCR

Perimeter leakage is not multiplied

Bulk leakage is multiplied, seeds avalanches

Typical PLI 25 um diameter SPAD, 293 K

Current (A)

1E-12 1E-11 1E-10 1E-9 1E-8 1E-7 1E-6 1E-5 1E-4

1 µW illumination

Photocurrent

Dark Current

Reverse Bias (V)

0 10 20 30 40 50

unmultiplied perimeter leakage

multiplied bulk leakage

optical input

anti-reflection coating

n-contact metallization

n'-InP substrate

i-InGaAsP grading

i-InP cap

n-InGaAsP buffer

n-InP charge

p'-InP diffused region

p-contact metallization

SiNx passivation
At low temperature, perimeter leakage dominates dark current up to breakdown

- Places upper limit on bulk dark carrier generation \((1.6 \times 10^{-19} \text{ A} = 1 \text{ e}^- \text{ per second})\)
- For 125 \(\mu\text{m}\) SPAD at 150 K, bulk leakage is probably 10X below perimeter leakage
  - probably have bulk carrier generation < \(10^4 \text{ e}^- \text{ per second} \sim 1 \text{ fA}\)

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**Data courtesy of Mike Krainak, NASA-Goddard**

more concerning these data from Mike Krainak, Tues. 12:00 talk
Structure Variations

- Epi-structure variations in thickness and doping
  - Variation in internal electric field profile at wafer edge
  - Allows for study of device performance as function of field profile
    (variation is generally bad for production, but can be good for R&D!)

![Graph showing breakdown voltage vs position](image-url)
SPAD performance: DCR vs DE

- Compare DCR vs DE for typical (T81x126) and edge (T80x144) devices
- T80x144 has superior performance for DCR vs DE
  - simulations indicate reduced E-fields in multiplication and absorption regions
  - leads to considerable trade-off in afterpulsing and jitter performance

![Graph showing DCR vs DE for T81x126 and T80x144 devices](graph.png)

- 25 µm diameter SPADs
- 200 K
- 200 ns gating
- active quenching
- 10 kHz repetition rate
Afterpulsing: DCR vs Hold-off Time $T_{\text{OFF}}$

- Dark count rate (DCR) increase at longer hold-off time $T_{\text{OFF}}$ indicates much stronger afterpulsing for edge device (P79x146).

Biasing scheme:
- 40 µm diameter SPADs
- 20 ns gating
- gated quenching
- ~5.5 V overbias
Model for Dark Carrier Generation

- Dark count generation due to several mechanisms
  - Primary dark carrier generated during gate pulse induces avalanche
    \[ N_{pdc} = \frac{I_{d,m} \tau}{q} \]
    - \( N_{pdc} \) = number of primary dark carriers
    - \( I_{d,m} \) = multiplied dark carriers
    - \( \tau \) = gate width
    - \( q \) = electron charge
  - Afterpulse dark carrier from exponential de-trapping of trapped carrier
    \[ N_{adc} = P_d N_{tr,0} \frac{e^{\frac{\tau}{\tau_d}} - 1}{e^{\frac{\Delta T}{\tau_d}} - 1} \]
    - \( N_{adc} \) = number of afterpulse dark carriers
    - \( P_d \) = total dark count probability
    - \( N_{tr,0} \) = number of initially filled traps
    - \( \tau_d \) = characteristic de-trapping time
    - \( \Delta T \) = time between gate pulses
  - Additional mechanisms related to dark carriers generated just before gate pulse (primary or afterpulse) - ignored in this analysis

Fitting for Characteristic De-trapping Time

- Use dark carrier generation model to fit for de-trapping time $\tau_d$
- Model predicts much sharper increase in DCR with shorter hold-off, but allows for reasonable estimate of $\tau_d$

![Graph showing dark count rate vs. hold-off time](image)

- solid lines: model
- points & dashed lines: experimental data

**Note:** Trap sites located in multiplication region.
Define normalized DCR: \( \text{DCR}_{\text{norm}} = \frac{\text{DCR}(T_{\text{off}})}{\text{DCR}(T_{\text{off}} = 1\text{ms})} \)

Hold-off time for fixed increase in \( \text{DCR}_{\text{norm}} \) scales with de-trapping time \( \tau_d \)
- \( T_{\text{off}} \) for \( \text{DCR}_{\text{norm}} = 10 \) \( \sim \) 4 \( \tau_d \)
- \( T_{\text{off}} \) for \( \text{DCR}_{\text{norm}} = 100 \) \( \sim \) 3 \( \tau_d \)
De-trapping Activation Energy

- Extract thermal activation energy $E_a$ for $T_{\text{off}}$ ($DCR_{\text{norm}} = 10$)
  - de-trapping time $\tau_d$ has same activation energy
- $E_a$ differs by $>2X$ for P79x101 and P79x146
  - both devices from same wafer - materials properties should be identical
- Results suggest that $E_a$ depends on E-field amplitude
  - de-trapping by thermally assisted tunneling
- Multiplication region optimization requires E-field balance
  - larger E for shorter $\tau_d$
  - smaller E for reduced tunneling
  - reduction of E for P79x146 calculated to be $<10\%$
DCR Activation Energy without Afterpulsing

- Determine DCR activation energy from DCR $\sim \exp(-E_a/kT)$
- Both devices show $E_a \sim 0.13$ eV for all overbias voltages
  - Small energy relative to $\varepsilon_g \sim 0.8$ eV bandgap of InGaAs
  - Karve et al. showed that $\varepsilon_g(T)$ for InAlAs multiplication region gives similar $E_a$, if InAlAs tunneling dominates DCR; but does not agree for InP
  - DCR exponential dependence on both $T$ and $V$ consistent with thermally assisted tunneling through shallow energy defects in bandgap

Karve, et al., APL 86, p. 63505 (2005)
Timing Jitter vs Overbias

- Jitter improves by order of magnitude with increased overbias
- Various contributions to jitter seems to dominated by interface trapping
- Lower interface fields for T80x144 lead to enhanced trapping resulting in larger jitter at 200K relative to T81x126
- Record lower jitter results (see talk given by Jim Vickers, Tues. 14:40)
Timing Jitter vs Temperature

- Timing jitter degrades significantly between 220 K and 175 K for device with lower interface field (P79x146)
- For larger interface fields, no sensitivity to temperature between 220 K and 175 K (P79x101)
Conclusions

- SPAD performance parameters are highly sensitive to internal electric field profiles arising from small structural variations.
- De-trapping activation energy for afterpulsing can change by >2X for 5 - 10% changes in multiplication region E-field.
- DCR activation energy of ~0.13 eV suggests thermally assisted tunneling through shallow defects.
- Timing jitter dominated by grading layer interface fields.
- Numerous design trade-offs to be managed:
  - In multiplication region: larger E for shorter $\tau_d$, smaller E for reduced tunneling.
  - At grading interface: larger E for low jitter, lower E for lower DCR.
    - At 200 K, achieved DCR ~ 4 kHz with DE ~ 25% at expense of jitter (~500 ps).
    - More typical performance of DCR ~ 20 kHz with DE ~ 25% and jitter ~ 100 ps.
  - Strong temperature dependences in most cases:
    - de-trapping times increase by 10X between 220 K and 150 K.
    - Jitter can increase by 5X between 220 K and 150 K.